Floating Gate Devices: Operation and Compact Modeling

by

Paolo Pavan
DII – Università di Modena e Reggio Emilia, Italy

Luca Larcher
DISMI – Università di Modena e Reggio Emilia, Italy

and

Andrea Marmiroli
STMicroelectronics, Central R&D, Italy

KLUWER ACADEMIC PUBLISHERS
NEW YORK, BOSTON, DORDRECHT, LONDON, MOSCOW

Contents

Contributing Authors ix

Preface xi

Foreword xv

1. INTRODUCTION 1

1. COMPACT MODELING 1
   1.1 General concepts and definitions 2
   1.2 The Compact Modeling of a Floating Gate Device 4
2. SEMICONDUCTOR MEMORIES 6
3. FLOATING GATE DEVICES 7
4. FIRST COMMERCIAL DEVICES AND PRODUCTS 9
5. EVOLUTION 10
6. APPLICATIONS AND MARKET CONSIDERATIONS 12
   6.1 Applications 12
   6.2 Market highlights 13

REFERENCES 14

2. PRINCIPLES OF FLOATING GATE DEVICES 17

1. TECHNOLOGY HIGHLIGHTS 17
   1.1 Introduction 17
   1.2 Lithography 18
   1.3 Field isolation 21
   1.4 Silicon oxidation 22
   1.5 Ion Implantation, Deposition, Etching, Chemical Mechanical Polishing, Metallization 22

2. CELL OPERATION 24
2.1 Charge injection mechanisms 24
2.2 Channel Hot Electron current 25
2.3 CHannel Initiated Secondary ELectron current 27
2.4 Fowler-Nordheim Tunneling Current 27
3. DISTURBS AND RELIABILITY 29
3.1 Programming Disturbs 30
3.2 Retention 30
3.3 Endurance 32
3.4 Erase Distribution 32
3.5 Scaling issues 33
REFERENCES 34

3. DC CONDITIONS: READ 37

1. TRADITIONAL FG DEVICE MODELS 37
1.1 The classical FG voltage calculation method 38
1.2 Drain current calculation 39
1.3 Limits of the capacitive coupling coefficient method 40
1.3.1 The capacitive coupling coefficient extraction procedure 41
1.3.2 The bias dependence of the capacitive coupling coefficients 42
2. THE CHARGE BALANCE MODEL 43
2.1 The Floating Gate voltage calculation procedure 45
2.2 Advantages and scalability 46
2.3 Parameter extraction 46
3. SIMULATION RESULTS 47
REFERENCES 54

4. TRANSIENT CONDITIONS: PROGRAM AND ERASE 57

1. MODELS PROPOSED IN THE LITERATURE 57
2. THE CHARGE BALANCE MODEL: THE EXTENSION TO TRANSIENT CONDITIONS 60
3. FOWLER-NORDHEIM CURRENT 61
3.1 Theory and compact modeling 61
3.1.1 Charge quantization effects on oxide barrier height 63
3.1.2 The oxide field calculation 65
3.2 Simulation Results 70
4. CHANNEL HOT ELECTRON CURRENT 74
4.1 Theory and Compact Modeling 74
4.1.1 The “lucky-electron” model 75
4.1.2 Alternative CHE current models 77
4.2 Simulation Results 80
4.3 CHISEL current modeling 82
REFERENCES 83

5. FURTHER POSSIBILITIES OF FG DEVICE COMPACT MODELS 87

1. RELIABILITY PREDICTION 87
   1.1 SILC impact on FG memory reliability 88
      1.1.1 SILC models proposed in the literature 89
   1.2 Examples of FG memory device reliability predictions: EEPROM data retention 91
2. STATISTICS 97

REFERENCES 99

6. NON VOLATILE MEMORY DEVICES 103

1. BASIC ELEMENTS 103
   1.1 Read biasing 104
   1.2 Program biasing 105
   1.3 Erase biasing 106
2. MAIN BUILDING BLOCKS OF THE DEVICE 107
3. MATRIX AND DECODERS 113
4. OPERATING MODES 116
   4.1 Read 116
   4.2 Redundancy Read 118
   4.3 Program 120
   4.4 Erase 120
5. DMA TEST 122

Acknowledgement 125

References 126

Acknowledgments 131